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10/596,944	06/29/2006	Robert Lee Maziasz	SC12656TS	2642

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EXAMINER	
SANDOVAL, PATRICK	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,944	MAZIASZ ET AL.	
	Examiner	Art Unit	
	PATRICK SANDOVAL	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-46 and 71-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-46 and 71-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed 4/5/2010. Claim 36 has been amended, claim 47 has been cancelled, and claim 79 has been added. Claims 36-46 and 71-79 are pending.

Response to Amendment

2. Applicant's arguments with respect to claims 36-47 and 71-78 have been considered but are moot in view of the new ground(s) of rejection in view of IDS reference Wolf, Wayne H. et al. (Wolf), "Algorithms for Optimizing Two-Dimensional Symbolic Layout Compaction", IEEE Transactions on Computer-Aided Design, Vol. 7, No. 4, April 1988, pp. 451-466 and previously relied upon prior art reference McGuinness et al. (McGuinness) (US2004/0078768).

Claim Objections

3. Claim 36 is objected to because of the following:

A. Lines 14-15 and 18-19 make reference to a third portion of a second transistor of the circuit layout, however there appears to be no prior reference to first and second portions of a second transistor of the circuit layout. As best understood by the Examiner, the claims were intended to refer rather to a third portion of the circuit layout, which is a first portion of a second transistor of the circuit layout.

B. Lines 21-22 make reference to a fourth portion of a second logical device, however there appears to be no prior reference to first through third portions of the second logical device. As best understood by the Examiner, the claims were

intended to refer rather to a fourth portion of the circuit layout, which corresponds to a portion of a second logical device in the circuit layout.

4. Examiner suggests clarification of claim 36 with regards to the above remarks for clarification regarding said third and fourth portions.

5. Claim 46 is objected to as it appears to be a redundant limitation with regards to independent claim 36 from which it depends. Examiner recommends deleting claim 46.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 36-46 and 71-79 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Pursuant to independent claim 36, line 2, and independent claim 79, line 2, regarding “during compaction of a circuit layout”, it is unclear if the remaining steps of claim 36, lines 4-22 and claim 79, lines 4-11, respectively, are also to take place during the compaction stage of a circuit layout.

9. As the first limitations of claim 36 and claim 79 presently stand, *the only thing that happens during compaction of a circuit layout is the determination at a computer device a first direction associated with the circuit layout.*

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 36-46 and 71-79 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Wolf, Wayne H. et al. (Wolf), "Algorithms for Optimizing Two-Dimensional Symbolic Layout Compaction", IEEE Transactions on Computer-Aided Design, Vol. 7, No. 4, April 1988, pp. 451-466 in view of McGuinness et al. (McGuinness) (US2004/0078768).

12. The applied reference McGuinness has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

13. Wolf discloses a non traditional method of two dimensional compaction of layouts through supercompaction algorithms, which analyze a layout to determine what changes will most improve the design (Wolf, Page 451, Section I). Supercompaction of Wolf involves geometric reorganization by moving components and wires (Wolf, Section V-A), wherein devices are able to be compacted in a preferred dimension by first pushing apart components (ie. "shearing") in a direction perpendicular to the preferred dimension. Components are moved in both x and y directions (Wolf, Fig. 7), wherein the y direction is a direction different than the x direction.

14. Wolf does not specifically disclose the incorporation of transistor folding into the compaction stages, wherein in response to, for example, reshaping a first portion of a first transistor to reduce a size of a first logical device in a first direction, a resultant second portion of the first logical device is also reshaped in response. Wolf similarly does not disclose wherein in response to, for example, reshaping a first portion of a second transistor to reduce a size of a second logical device in a second direction that is different than the first direction, a resultant second portion of the second logical device is also reshaped in response.

15. McGuinness discloses a transistor folding solutions list wherein each fold solution has a determined minimum cell height HLB and minimum cell width WLB that may be provided by each particular fold solution (McGuinness, Paragraphs 36-37), wherein fold solutions may be modified as necessary through finger size redistribution/shortening/lengthening for layout accommodation of, for example, target cell height boundaries (McGuinness, Paragraphs 47-48, wherein reduction of one finger size height of a folded transistor is compensated by increases in other finger sizes). In example fold solutions for specific transistor sizing, transistor fingers are provided in Figs. 10-14 of McGuinness exemplifying the redistribution/shortening/lengthening of transistor fingers as deemed necessary to accommodate other layout objects (McGuinness, See Figs. 10, 11, 12, 13, 14, and applicable text wherein for example, transistor NTx2 is implemented by either 2 or 3 fingers, transistor NTx1 is implemented by either 1 or 2 fingers, transistor PTx2 is implemented by either 1 or two fingers). The fold solutions shown in Figs. 11-13 *vary both in overall transistor cell layout width and*

height dependent on choice of finger size/quantity, and thus transistor portions are reshaped/resized both in a first direction and a second direction different from the first direction. A design with more fingers may be shorter in transistor cell height, but wider as a result (and vice versa). Transistor fold solution variants are important in McGuinness, because although McGuinness recites the importance of meeting cell height, McGuinness also discloses an importance on finding a solution with smallest cell width that meets required cell height constraints (McGuinness, Paragraph 28). *Thus McGuinness is concerned with both layout height and width.*

16. Although McGuinness doesn't explicitly disclose incorporation of folding/unfolding in the compaction stage to modify transistor height/width so as to reduce layout height/width, it would have been obvious that the incorporation of finger modification within compaction stages *would provide further flexibility* for design layout modification/compaction. McGuinness already discloses the knowledge of finger modification for purposes of width and height sizing, and it would have been obvious to one of ordinary skill in the art that further incorporating the finger modification/redistribution of McGuinness into layout compaction stages would further address issues of expansion of layout height and width that may have resulted from, for example, small object placement and routing prior to compaction (McGuinness, Fig. 2 #'s 32, 36, 38, 40 and 42 and applicable text).

17. Wolf in view of McGuinnes thus discloses:

18. (Claims 36, 46 and 79) A method comprising:

during compaction of a circuit layout, (McGuinness' transistor folding to meet height/width constraints of Paragraphs 28, 36-37, 47-48, Figs. 2 and 10-14 incorporated into the supercompaction of Wolf, wherein reduction of one finger size height of a folded transistor is compensated by increased height in other finger sizes) selecting at the computer device a first portion of a first transistor of the circuit layout in response to determining the first portion extends outward in a first direction from a first logical device of the circuit layout, the first logical device comprising the first transistor, and in response to selecting the first portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction (McGuinness, Fig. 10 and Fig. 11 #'s 320-324, wherein of first transistor PTx1, *finger W=20 of PTx1 is reduced to 10* (ie. reshaped first portion) in the layout of PTx1, and an additional finger with W=10 is created to reduce overall W of the inverter formed);

reshaping at the computer device a second portion of the first logical device in response to reducing the size of the first logical device (McGuinness, Fig. 10 and Fig. 11 #'s 320-324, wherein of first transistor PTx1, finger W=20 of PTx1 is reduced to 10 in the layout of PTx1, and *an additional finger with W=10 is created* (ie. reshaped second portion) to reduce overall W of the inverter formed);

similarly reducing the size of a second logical device in a second direction different than the first direction by reshaping a third portion of the second logical device (McGuinness, Paragraphs 47-48, wherein addition/deletion of a transistor finger, affects transistor cell layout width, and ultimately reduces/increases transistor cell height, Fig.

12, wherein variations of second transistor NTx2, transistor cell layout width is reduced by modifying NTx2 from 3 fingers of W=6.7 to 2 fingers of W=10); and

reshaping at the computer device a fourth portion of the second logical device in the second direction in response to reducing the size of the second logical device in the second direction (McGuinness, Fig. 12, wherein variations of second transistor NTx2, transistor cell layout width is reduced by modifying NTx2 from 3 fingers of W=6.7 to 2 fingers wherein their respective W=10).

19. (Claim 37 and 71) Wherein the first portion of the first transistor comprises a first transistor finger, and the third portion of the second transistor comprises a first transistor finger (McGuinness, Paragraphs 47-48, Paragraph 57, Figs. 10-13).

20. (Claim 38 and 72) Wherein the second portion of the first logical device comprises a second transistor finger of the first transistor and wherein the fourth portion of the second transistor comprises a second transistor finger of the second transistor (McGuinness, Paragraphs 47-48, Paragraph 57, Figs. 10-13).

21. (Claim 39 and 73) Wherein the second portion of the first logical device comprises a transistor finger of a second transistor and wherein the fourth portion comprises a transistor finger of a third transistor (McGuinness, Paragraphs 47-48, Paragraph 57, Figs. 10-13).

22. (Claims 40, 74 and 78) Wherein reshaping the first/third portion comprises reducing a size of the first transistor finger (McGuinness, Paragraphs 47-48, finger size reduction, Paragraph 57, Figs. 10-13).

23. (Claims 41 and 75) Wherein reshaping the first/third portion comprises removing the first transistor finger (McGuinness, Paragraphs 47-48, wherein reduction of one finger size height of a folded transistor is compensated by increases in other finger sizes, Paragraph 57, Figs. 10-13).

24. (Claims 42 and 76) Wherein reshaping the first/third portion comprises rotating the first transistor (wherein layout/cell compaction it is well known to rotate/move/alter ratios/shapes as needed to improve the overall layout area).

25. (Claims 43 and 77) Reshaping a third portion of the first logical device in response to reducing the size of the first transistor portion (McGuinness, Paragraphs 47-48, wherein reduction of one finger size height of a folded transistor is compensated by increases in other finger sizes, Paragraph 57, Figs. 10-13).

26. (Claims 44 and 45) Storing a first state associated with the circuit layout at the computer device in response to selecting the first portion of the first transistor; in response to reshaping the first portion of the first transistor, determining if a size of the circuit layout has been reduced in the first direction (McGuinness, Paragraphs 26 and 29, Fig. 2, wherein each fold solution is selected and used in turn to generate a possible layout to generate a final optimized cell layout solution, wherein layout height is compared to cell height constraint); and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state (McGuinness, Paragraph 29, wherein the best optimized layout is chosen) (wherein it is inherent in layout optimization that if a proposed solution does not meet cell height constraints it would not be a valid solution).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICK SANDOVAL whose telephone number is (571)272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Patrick Sandoval/
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